REMARKS/ARGUMENTS

In the Office Action mailed May 14, 2009, claims 1-20 were rejected. In response, Applicants hereby request reconsideration of the application in view of the amendments and the below-provided remarks. Claims 1-2, 5, 7-9, 12, 15, and 19-20 are amended. No claims are added or canceled.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-2, 5, 8-9, and 12 were rejected under 35 U.S.C. 102(b) as being anticipated by Imai (U.S. Pat. No. 5,506,427). Additionally, claims 3 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Koshimizu et al. (U.S. Pat. Pub. No. 2005/0181569 A1, hereinafter Koshimizu). Additionally, claims 4, 11, 15, and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Schiz et al. (Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy, IEEE Transactions on Electron Devices, Vol. 48, No. 11, November 2001, hereinafter Schiz). Additionally, claims 6 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Verma et al. (U.S. Pat. Pub. No. 2005/0079678 A1, hereinafter Verma). Additionally, claims 7 and 14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Imai in view of Frei et al. (U.S. Pat. No. 6,509,242 B2, hereinafter Frei). Additionally, claim 16 was rejected under 35 U.S.C. 103(a) as being unpatentable over Imai and Schiz, and further in view of Koshimizu. Additionally, claim 18 was rejected under 35 U.S.C. 103(a) as being unpatentable over Imai and Schiz, and further in view of Verma. Additionally, claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over Imai and Schiz, and further in view of Frei. Additionally, claim 20 was rejected under 35 U.S.C. 103(a) as being unpatentable over Imai and Schiz, and further in view of Asai et al. (U.S. Pat. No. 6,455,364 B1, hereinafter Asai). However, Applicants respectfully submit that these claims are patentable over Imai, Koshimizu, Schiz, Verma, Frei, and Asai for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to particularly point out that the second silicon layer forms a second mono-crystalline layer over the first mono-crystalline layer. As amended, claim 1 recites:

> "A method for growing a mono-crystalline emitter for a bipolar transistor, comprising:
>
> providing a trench formed on a silicon substrate having opposed silicon oxide side walls;
>
> selectively growing a highly doped mono-crystalline layer on the silicon substrate in the trench; and
>
> non-selectively growing a second silicon layer over the trench in order to form an amorphous or polysilicon layer over the silicon oxide sidewalls and a second mono-crystalline layer over the first mono-crystalline layer" (emphasis added).

In contrast, Imai does not disclose non-selectively growing a second silicon layer over the trench. In fact, the cited portion of Imai (col. 4, lines 48-50) merely discloses that an emitter electrode of n^+-type polysilicon is formed on the intrinsic base, but does not disclose that this emitter electrode is formed by "non-slectively growing a second silicon layer," as recited in claim 1. The cited portion of Imai (col. 4, lines 48-50) further discloses that the emitter electrode is annealed in order to form an n-type emitter by diffusion of the dopant. Even if forming the emitter electrode on the intrinsic base, as disclosed in the cited portion (Imai, col. 4, lines 48-50), were understood to disclose growing a second silicon layer over the trench, in general, Imai nevertheless fails to disclose that the second silicon layer forms a layer over the first mono-crystalline layer, as recited in claim 1, because Imai discloses that the emitter electrode is annealed to form the n-type emitter.

Furthermore, Imai does not disclose that a second silicon layer forms an amorphous or polysilicon layer over the silicon oxide sidewalls and a second mono-crystalline layer over the first mono-crystalline layer. Rather, Imai discloses that an emitter electrode of n^+-type polysilicon is formed on the n^+-type emitter (Imai, col. 4, lines 16-17. Emphasis added). The step of forming an n^+-type polysilicon electrode on the n^+-type emitter is different from forming a second mono-crystalline layer over the first mono-crystalline layer, because the electrode as disclosed by Imai is a polysilicon layer, not a mono-crystalline layer, as recited in claim 1. Furthermore, Imai does not disclose forming an amorphous or polysilicon layer over the silicon oxide sidewalls.

Rather, Imai merely discloses that the emitter electrode is formed on the n^+-type emitter (Imai, col. 4, lines 16-17).

For the reasons presented above, Imai does not disclose all of the limitations of the claim because Imai does not disclose non-selectively growing a second silicon layer over the trench in order to form an amorphous or polysilicon layer over the silicon oxide sidewalls and a second mono-crystalline layer over the first mono-crystalline layer, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is not anticipated by Imai, because Imai does not disclose all of the limitations of the claim.

Independent Claim 8

Applicants respectfully assert independent claim 8 is not anticipated by Imai at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 8 recites "non-selectively growing a second silicon layer over the silicon substrate and silicon oxide to form a second mono-crystalline layer over the silicon substrate and an amorphous or polysilicon layer over the silicon oxide" (emphasis added).

Here, although the language of claim 8 differs from the language of claim 1 and the scope of claim 8 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 8. Accordingly, Applicants respectfully assert claim 8 is not anticipated by Imai because Imai does not disclose "non-selectively growing a second silicon layer over the silicon substrate and silicon oxide to form a second mono-crystalline layer over the silicon substrate and an amorphous or polysilicon layer over the silicon oxide," as recited in claim 8.

Independent Claim 15

Applicants respectfully assert independent claim 8 is not anticipated by Imai at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 15 recites "growing a second layer over the trench using differential epitaxial growth in order to form an amorphous or polysilicon layer over the

silicon oxide sidewalls and a mono-crystalline layer over the highly doped layer" (emphasis added).

Here, although the language of claim 15 differs from the language of claim 1 and the scope of claim 15 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 15. Accordingly, Applicants respectfully assert claim 15 is not anticipated by Imai because Imai does not disclose "growing a second layer over the trench using differential epitaxial growth in order to form an amorphous or polysilicon layer over the silicon oxide sidewalls and a mono-crystalline layer over the highly doped layer," as recited in claim 15.

Dependent Claims 2-7, 9-14, and 16-20

Claims 2-7. 9-14, and 16-20 depend from and incorporate all of the limitations of the corresponding independent claims 1, 8, and 15. Applicants respectfully assert claims 2-7. 9-14, and 16-20 are allowable based on allowable base claims. Additionally, each of claims 2-7. 9-14, and 16-20 may be allowable for further reasons, as described below.

In regard to claims 4 and 11, Applicants respectfully submit that claims 4 and 11 are patentable over the combination of Imai and Schiz because the combination of cited references does not teach or suggest all of the limitations of the claims. Claims 4 and 11 recite that the "step of non-selectively growing the second silicon layer is accomplished using differential epitaxial growth" (emphasis added). In contrast, Imai does not disclose the step of non-selectively growing the second silicon layer. In fact, Imai merely discloses that an emitter electrode is formed on the n^+-type emitter, but does not disclose that this step includes non-selectively growing the second silicon layer, as recited in claims 4 and 11.

Accordingly, Applicants respectfully assert that claims 4 and 11 are patentable over Imai and Schiz because Imai does not disclose the "step of non-selectively growing the second silicon layer," as recited in claims 4 and 11.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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